

ASA-1003

TRANSMITTAL LETTER TO THE UNITED STATES
DESIGNATED/ELECTED OFFICE (DO/EO/US)

U.S. APPLICATION NO. (if known, see 37 CFR 1.5)

09/856758

International Application No.

PCT/JP99/06595

International Filing Date

November 26, 1999

Priority Date Claimed

November 30, 1998

Title of Invention **METHOD OF MOUNTING ELECTRONIC CIRCUIT CHIP**

Applicant(s) for DO/EO/US **C. OKAMOTO et al (see attached)**

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. This is a FIRST submission of items concerning a filing under 35 U.S.C. 371.
2. This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. 371.
3. This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. A copy of the International Application as filed (35 U.S.C. 371(c)(2))
 - a. is transmitted herewith (required only if not transmitted by the International Bureau).
 - b. has been transmitted by the International Bureau.
 - c. is not required, as the application was filed in the United States Receiving Office (RO/US).
6. A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
 - a. are transmitted herewith (required only if not transmitted by the International Bureau).
 - b. have been transmitted by the International Bureau.
 - c. have not been made; however, the time limit for making such amendments has NOT expired.
 - d. have not been made and will not be made.
8. A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
12. An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
13. A FIRST preliminary amendment.
 A SECOND or SUBSEQUENT preliminary amendment.
14. A substitute specification.
15. A change of power of attorney and/or address letter.
16. Other items or information:

[X] THIS APPLICATION IS BEING FILED WITHOUT AN EXECUTED DECLARATION, WHICH WILL BE FILED LATER.

[x] LIST OF INVENTORS' NAMES AND ADDRESSES.

U.S. PATENT AND TRADEMARK OFFICE

U.S. Application No. (if known) 097856758 International Application No. PCT/JP99/06595	Attorney's Docket Number ASA-1003
--	---

17. The following fees are submitted:

	CALCULATIONS	PTO USE ONLY
<u>Basic National Fee (37 CFR 1.492 (a)(1)-(5)):</u>		
Search Report has been prepared by the EPO or JPO	\$860.00	
International preliminary examination fee paid to USPTO (37 CFR 1.482)	\$690.00	
No international preliminary examination fee (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445 (A)(2))	\$710.00	
Neither international examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(A)(2)) paid to USPTO	\$1000.00	
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2) to (4)	\$100.00	

ENTER APPROPRIATE BASIC FEE AMOUNT = \$ 860.00

Surcharge of \$130.00 for furnishing the oath or declaration later than 20 30 months from the earliest claimed priority date (37 CFR 1.492(e)). + \$ 130.00

Claims	Number Filed	Number Extra	Rate		
Total	14 - 20 =	0	x \$18.00	\$	0.00
Independent	7 - 3 =	4	x \$80.00	\$	320.00
Multiple dependent claim(s) (if applicable)				+ \$270.00	\$ 0.00
TOTAL OF ABOVE CALCULATIONS				=	\$ 1,310.00

Reduction by 1/2 for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 CFR 1.9, 1.27, 1.28). \$ 0.00

SUBTOTAL = \$ 1,310.00

Processing fee of \$130.00 for furnishing the English translation later than 20 30 months from the earliest claimed priority date (37 CFR 1.492(f)). + \$ 0.00

TOTAL NATIONAL FEE = \$ 1,310.00

Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31). \$40.00 per property. + \$ 0.00

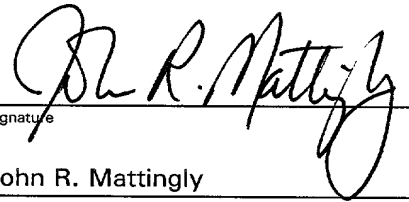
TOTAL FEES ENCLOSED = \$ 1,310.00

	Amount to be:
	Refunded \$
	Charged \$

- a. A check in the amount of \$ 1,310.00 to cover the above fees is enclosed.
- b. Please charge my Deposit Account No. 50-1417 in the amount of \$ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.
- c. The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-1417. A duplicate copy of this sheet is enclosed.

Note: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:
 MATTINGLY, STANGER & MALUR, P.C.
 104 East Hume Avenue
 Alexandria, Virginia 22301
 (703) 684 -1120



 Signature
 John R. Mattingly

 Name



30,293

 Registration Number

PCT/JP99/06595

6/PRTS

09/856758

E5885
26/14

1

531 Rec'd PCT/T

25 MAY 2001

DESCRIPTION

METHOD OF MOUNTING ELECTRONIC CIRCUIT CHIP

TECHNICAL FIELD

The present invention relates to a technology of mounting an electronic circuit chip such as an integrated circuit chip onto a soft material such as paper.

TECHNICAL BACKGROUND

These years, electronic circuit chips such as integrated circuit chips have become thinner and thinner, and accordingly, the electronic circuit chips have been used in various configurations.

In a use condition of such an electronic circuit chip, for example, as disclosed in Japanese Laid-Open Patent No. H3-38396, a small-sized electronic circuit chip for storing data is embedded in a portable plastic card together with an element for reading data in a noncontact manner. For example, such a plastic card that personal identification data has been previously stored in the electronic circuit chip, can be used as an electronic ID card which can confirm personal identification data in a noncontact manner.

09558560

DISCLOSURE OF INVENTION

The use configuration of the above-mentioned electronic circuit chip have become prosperous. However, conventionally, materials to which electronic circuit chips are mounted have been limited to materials such as plastic cards which are hard so that it cannot be largely bent and folded. It is because if a force which can largely bend or fold the materials is exerted to the materials, the electronic circuit chips are possibly damaged due to the reason of strength thereof.

However, if an electronic circuit chip can be mounted to a material such as paper which can be largely bent or folded, the use configuration of the electronic circuit chip can be broadened, and higher convenience becomes available for people.

Accordingly, an object of the present invention is to provide a mounting method with which an electronic circuit chip is prevented from being damaged even though a soft material on which the electronic circuit chip is mounted is bent or folded.

Further, another object of the present invention is to provide an electronic circuit chip which cannot be damaged even through a soft material such as paper on which the electronic circuit chip is mounted is bent or folded.

To the end, according to the present invention, there is provided a method of mounting an

TOSTER "B529360

electronic circuit chip onto a foldable sheet, wherein during mounting, the electronic circuit chip is prevented from being located at a position where the sheet creates a crease when it is folded in a predetermined folding manner. With this mounting method, the electronic circuit chip is located while it is avoided from being mounted at a position of a crease to which a high moment force is exerted upon folding of the sheet, thereby it is possible to prevent the electronic circuit chip from being damaged by folding the sheet.

Further, with the use of parameters required for an electronic circuit chip to be mounted on the above-mentioned sheet, a specification for the electronic circuit chip, which can prevent occurrence of damage to the electronic chip even though the sheet is folded, is provided.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a circuit diagram illustrating a circuit using an electronic circuit chip which is mounted on paper in an embodiment of the present invention;

Figs. 2a and 2b are views illustrating such a condition that a circuit using an electronic circuit chip in a first embodiment of the present invention is mounted on paper;

Figs. 3a and 3b are views illustrating a such

0988758-091501
"05160" 85298860

condition that a circuit using an electronic circuit chip is mounted on paper in a second embodiment of the present invention;

Figs. 4a to 4d are sectional views illustrating such conditions that an electronic circuit chip are mounted on paper in a third embodiment of the present invention;

Fig. 5 is a view which approximately exhibits a force and a moment exerted so as to curve the electronic circuit chip in the third embodiment of the present invention, and

Fig. 6 is a view illustrating a tape on which electronic circuit chips are mounted.

Best Mode For Carrying Out The Invention

Explanation will be made hereinbelow of embodiments of the present invention.

In the following explanation of the embodiments according to the present invention, there is exemplified in such a configuration that an electronic circuit chip for storing data is mounted on a paper together with an element for reading the data from the electronic circuit chip in a noncontact manner. However, it is noted that an electronic circuit chip to be mounted may be any of those other than that mentioned above, and further, any of soft materials other paper on which the electronic circuit chip is mounted may be used if it may be largely bent

FOR "B579560"

or it may be folded.

Further, a thin and laterally very long sheet such a tape may be used other than a planer material. That is, it may be the one which can be rolled-up.

5 Explanation will be made of a first embodiment of the present invention.

Referring to Fig. 1 which shows a circuit composed of an electronic circuit chip adapted to be mounted on a paper in this embodiment, and an element
10 for reading data from the electronic circuit chip in a noncontact manner, there is shown an electronic circuit chip 1 in which electronic circuits are integrated on a silicon chip. Further, elements, that is, a capacitor 2 and an antenna 3 are elements for reading data from
15 the electronic circuit chip 1 in a noncontact manner.

When an electromagnetic wave is applied to the above-mentioned circuit from the outside, the electromagnetic wave induces a current running through the capacitor through the antenna 3, and a power is
20 charged in the capacitor 2. Further, the power charged in the capacitor causes the electronic circuit 1 to be energized so that data previously stored is transmitted in the form of an electromagnetic wave from the antenna 3. Accordingly, through the application of an
25 electromagnetic wave, the data stored in the electronic circuit chip can be read on the outside thereof in a noncontact manner.

Fig. 2a shows a condition in which the

circuit is mounted on paper, reference numeral 200 denotes the outer surface of a sheet on which the circuit is mounted. In the figure, reference numerals 210a to 210d denote configuration examples of the
5 circuits which are mounted on a paper sheet.

It is noted here that the circuit 210d is bonded so as to be held between two sheets 400, 401 (201, 203) or a circuit 210d is bonded to a rear surface of a paper sheet 500.

10 Further, the circuit is mounted on the paper sheet in such a configuration that the electronic circuit chip is prevented from being mounted at a position on a crease which is created in the paper sheet, as indicated by a one-dot chain line, and a two-
15 dot chain line in the top view 200, when the paper sheet is folded. This figure shows such an example that the paper sheet is possibly folded into 1/2, 1/3 or 1/4 in the lateral direction thereof, and is possibly folded into 1/2 or 1/4 in the longitudinal
20 direction. The one-dot chain lines and the two-dot chain lines in the figure exhibit creases when the paper sheet is folded as mentioned above.

A position where a crease is possibly created so that the electronic circuit chip 1 is not located, is a
25 position in accordance with a configuration of folding if the configuration of folding has been previously known. Further, if no configuration with which the paper is folded are previously known, a position which

is one or a plurality of configurations which are usually used in various paper folding methods in accordance with kinds or uses of the paper sheet. That is, in general, the position may be on a crease which is created at any of positions obtained by $1/n$ of the length of the paper sheet, where n is an integer, that is, in general 2, 3, 4, 5, 6, 8, 16 in both vertical and horizontal directions, that is, positions which are $1/2$, $1/3$, $1/4$, $1/6$, $1/8$, $1/16$ of the length of the paper sheet in each of the longitudinal and lateral directions, where a crease is possibly created, except a special kind or use of the paper sheet.

By locating the electronic circuit chip on the paper sheet, other than a position where a crease is created and where a large moment force is exerted when the paper sheet is folded, it is possible to prevent the electronic circuit chip 1 from being damaged when the paper sheet is folded.

It is noted that the circuit 210a is arranged so that the electronic circuit chip 1 is located at a position in the vicinity of an edge of the paper sheet. Usually, since no large force is exerted to a position in the vicinity of an edge of the paper sheet, a degree of the force exerted to the electronic circuit chip 1 and the frequency of the exertion of the force to the electronic circuit chip 1 can be expected to be less. Alternatively, in such a case that concavities and convexities are impressed to the paper sheet for blind

persons so that hard parts are formed, the electronic circuit chip 1 may be located in any of these parts since it may be expected to decrease the force exerted to the electronic circuit chip 1 located in this part.

5 Further, in such a case that an antenna 3 which has a strait-line like shape as a whole, as in this embodiment, the circuit is arranged so that the antenna 3 is located in parallel with a side of the paper sheet as in the configuration examples 210a to 10 210d. Usually, the paper sheet is bent or folded in parallel with a side of the paper sheet, and accordingly, a degree of a force exerted to the antenna 3 and the frequency of exertion of forces exerted to the antenna 3 can be expected to be less.

15 Further, the upper bottom surface (which is a surface in parallel with the surface) of the sheet of the electronic circuit chip 1 which is weak against a force in the bending direction, is designed so as to have a small size in order to prevent the electronic 20 circuit chip from being exerted thereto with a large bending moment.

Further, as shown in Fig. 2b which is an enlarged view illustrating a circuit, the electronic circuit chip 1 is located on a capacitor 2 which is 25 formed so that its upper bottom surface (which is in parallel with the surface of the paper sheet) is larger than the electronic circuit chip 1, and accordingly, the upper bottom surface of the electronic circuit chip

is accommodated within the upper bottom surface of the capacitor 2 as viewed in a direction perpendicular to the surface of the paper sheet. With this arrangement, the capacitor 2 can protect the electronic circuit chip 1 from a force externally exerted. It is noted that if the upper bottom surface of the electronic circuit chip 1 is accommodated within the upper bottom surface of the capacitor 2 as viewed in a direction perpendicular to the surface of the paper sheet, the circuit may have such a structure that the antenna 3 is located between the capacitor 2 and the electronic circuit chip 1.

Explanation will be hereinbelow made of a second embodiment. Refereeing to Figs. 3a and 3b which top views illustrating examples of configurations of circuits mounted on paper sheets, and in which 310a to 310d exhibit examples of configurations of circuits which are mounted on the paper sheets. The circuit is held between two sheets 400, 401 to which the circuit is bonded, similar to the first embodiment, as exhibited by a circuit 301d (301, 303). Alternatively, the circuit 310d is mounted being bonded to the rear surface of a paper sheet 500.

It is noted here that in the second embodiment, the capacitor 2 is manufactured, having a strength with which the capacitor cannot be folded. Further, as shown in the figures, the upper bottom surface (which is in parallel with the surface of the paper sheet) of the capacitor is set to a size which is

slightly smaller than each of lattice spaces defined by section lines (one-dot chain lines shown in the figures) for sectioning the paper sheet in both longitudinal and lateral directions by $(1/n)$ where n is an integer, and the sides of the paper sheet (the shape of each grid is not always rectangular), and the capacitor 2 is located at the center of any one of the lattice spaces.

In the example as shown, the lattice spaces are defined by section lines (one-dot chain lines as shown in the figure) sectioning the paper sheet into $1/2$ in the longitudinal direction, and sectioning the paper sheet into $1/4$ in the lateral direction, and the sides of the paper sheet. The section lines defining the lattice spaces are set so that the creases in a certain folding configuration become the section lines if this folding configuration has been previously known. Further, if no folding configuration has not previously known, creases which are created in one of folding configurations which are usually used in accordance with a kind or use of the paper sheet are set as the section lines. That is, other than a special kind or use of the paper sheet, the positions of the section lines defining the lattice spaces are set at every $1/2$, $1/3$, $1/4$, $1/6$, $1/8$ or $1/16$ of the length of the paper sheet in either of the lateral and the longitudinal directions.

Further, in the second embodiment, as shown

FOR FILED IN 35293860

in Fig. 3b which is an enlarged view illustrating the circuit, the electronic circuit chip 1 is arranged on the capacitor which is manufactured so that its upper bottom surface (which is in parallel with the surface of the paper sheet) is larger than the electronic circuit chip 1, and accordingly, the upper bottom surface of the electronic circuit chip 1 is accommodated within the upper bottom surface of the capacitor 2 as viewed in a direction perpendicular to the surface of the paper sheet. With this arrangement, the capacitor 2 can protect the electronic circuit chip 1 against a force externally exerted. It is noted that if the upper bottom surface of the electronic circuit chip 1 is accommodated within the upper bottom surface of the capacitor 2 as viewed in a direction perpendicular to the surface of the paper sheet, the circuit may have such a structure that the antenna 3 is located between the capacitor 2 and the electronic circuit chip 1.

According to the second embodiment configured as mentioned above, since the paper sheet can hardly be folded in the part occupied by the capacitor 2, it can be expected that the paper sheet is never folded in the part occupied by the capacitor 2. Thus, the electronic circuit chip 1 located in the part occupied by the capacitor 2 can be expected to be prevented from being exerted thereto with a strong force externally applied. Further, the capacitor 2 is located at a position which

does not hinder the folding of the paper sheet in a usual configuration, and accordingly, it is possible to present the convenience of the use of the paper from being greatly laurel.

5 Explanation will be hereinbelow made of a third embodiment of the present invention.

In the case of mounting the electronic circuit chip on a paper sheet, when a force is exerted to the paper sheet from the outside due to handling of
10 the paper sheet, the force is also exerted to the paper sheet when the paper sheet is curved. In this embodiment, if the electronic circuit chip is planar (in a nearly rectangular parallelepiped), the electronic circuit chip which is designed satisfying
15 conditions having been previously obtained in order to prevent the electronic circuit chip from being broken by a force externally exerted is mounted on the paper sheet.

Referring to Figs. 4a to 4d, there are shown
20 electronic circuit chips 41 and paper sheets 42, 43. Figs. 4a and 4c show an example in which the electronic circuit chip 41 is held between the sheets 42, 43 which are bonded together, Fig. 4a illustrating a condition in which no force is exerted to the paper sheet while
25 Fig. 4c illustrates a condition in which a force is exerted to the paper sheet which is therefore curved. Figs. 4b and 4d show in an example in which the electronic circuit chip 41 is bonded to the upper

surface of the paper sheet 43, Fig. 4b illustrating a condition in which no force is exerted thereto while Fig. 4d illustrates a condition in which a force is exerted thereto so that the paper sheet is curved.

5 When a force and a moment are exerted to the paper sheet so that the long sides of the planar surface of the electronic circuit chip are curved, the force and the moment are effected in various positions on the electronic circuits chip. Estimating that one
10 of the short sides of the planar surface of the electronic circuit chip is set as a fixed end while the other side on the opposite side is set as a free end, the force and the moment can be exhibited being substituted by the equally distributed loads exerted
15 over the entire area of the planar surface, a concentrated load exerted to the free end, and a moment exerted to the free end. Even in such a case that the electronic circuit chip is held between the paper sheets, and also in such a case that it is bonded to
20 the upper surface of the paper sheet, it is approximated to a similar configuration.

Referring to Fig. 5 which is a view approximately exhibits a force and a moment which are exerted so as to curve the electronic circuit chip, a
25 part indicated by rightward upward oblique lines exhibits a section of the electronic circuit chip 41, in parallel with the long sides of the planer surface thereof. The short sides of the planar surface of the

electronic circuit chip 41 correspond to opposite ends of the section of the electronic circuit chip 41 in Fig. 4. Of these ends, the left end serves as the free ends while the right end serves as the fixed end.

5 Referring to Fig. 4, the fixed part is exhibited by rightward downward oblique lines. Referring to this figure, there are shown a thickness H (m) of the electronic circuit chip 41, the length L (m) of the long sides of the electronic circuit chip, equally
 10 distributed loads P (N/m^2) per unit area, which are exerted over the entire area of the planar surface of the electronic circuit chip 41, a concentrated load W (N/m) per unit length, exerted to the free end, and a bending moment M (N) per unit length, exerted to the
 15 free end.

The forces P and W and the moment M with which the electronic circuit chip 41 is curved, are estimated to be exerted within the section thereof, and a positive force or moment is taken in a direction in
 20 which the electronic circuit chip 41 is curved downward. In this embodiment the forces P and W and the moment M have positive values.

The x -axis is taken rightward from the free end as the origin. A moment per unit length, exerted
 25 to a position x (m) by the equally distributed loads P , is exhibited by $Px^2/2(N)$. A moment per unit length, exerted to a position x (m) by the concentrated load W is exhibited by Wx (N). A moment per unit length

exerted by the bending moment M is exhibited by a constant value $M(N)$, independent from the value x .

Accordingly, the total value M_{SUM} of the moments per unit length, exerted to the position x (m) is exhibited by
 5 $Px^2/2 + Wx + M(N)$. x is taken in a range from 0 to L , and accordingly, M_{SUM} becomes maximum at $x = L$, thus,

$$M_{MAX} = PL^2/2 + WL + M(N)$$

is obtained.

In this embodiment, since the shape of the
 10 electronic circuit chip can be approximated to a rectangular parallelepiped body, the bending stress exerted to the electronic circuit chip 41 becomes maximum at a position where the maximum bending moment is exerted, having a value σ_{MAX} becomes $6M_{MAX}/H^2(N/m^2)$.

15 If the bending strength of the electronic circuit chip 41 is denoted by σ (N/m_2), since a condition with which the electronic circuit 41 can be prevented from being broken, is $\sigma \geq \sigma_{MAX}$,

$$3PL^2 + 6WL + 6M - \sigma H^2 \leq 0 \quad \dots \text{(Formula 1)}$$

20 is obtained.

By solving the equation for L , H , σ ,

$$L \leq \{-W + (W^2 - PA)^{1/2}\}/P \quad \dots \text{(Formula 2)}$$

$$H \geq \{3(PL^2 + 2WL + 2M)/\sigma\}^{1/2} \quad \dots \text{(Formula 3)}$$

$$\sigma \geq (3PL^2 + 6WL + 6M)/H^2 \quad \dots \text{(Formula 4)}$$

25 are obtained. In the formula 2, A is $A = 2M - \sigma H^2/3$.

As a condition with which the electronic circuit chip is prevented from being broken, the maximum value of the length L (m) of the long sides is

obtained from the formula 2, the minimum value of the thickness H (m) is obtained from the formula 3, and the minimum value of the bending strength σ (N/m^2) is obtained from the formula 4.

5 In an example, in such a case that the electronic circuit chip is mounted between the paper sheets, having a thickness with which the electronic circuit chip cannot be recognized even though the paper sheets are externally touched, the maximum thickness H 10 (m) of the electronic circuit chip is determined. By substituting a bending strength σ (N/M^2) which can be obtained from the material quality and the shape of the electronic circuit chip, the equally distributed loads P (N/m^2) per unit area and the concentrated load $W(N/m)$ 15 per unit length which are expected to be applied when paper is used, and the moment M (N) per unit length, into the formula 2, the maximum long side length L (m) with which the electronic circuit chip can be prevented from being broken can be obtained.

20 In another example, in such a case that the electronic circuit chip should have multiple functions, since the scale of the circuit becomes larger, the minimum value of the long side length L of the electronic circuit chip is determined. By substituting 25 a bending strength σ (N/m^2), the equally distributed loads P (N/m^2) per unit area, and the concentrated load $W(N/m)$ per unit length, and the moment M (N) per unit length, which are obtained similar to those as

mentioned above, into the formula 3, the minimum thickness H (m) with which the electronic circuit chip can be prevented from being broken, can be obtained.

Thus, according to this embodiment, it is possible to provide an electronic circuit chip which can be prevented from being broken even though it is mounted to a soft material such as paper. Further, it is possible to provide a sheet on to which the electronic circuit chip designed as mentioned above is mounted.

Next, explanation will be hereinbelow made of a forth embodiment of the present invention.

In this embodiment, a tape like sheet on which electronic circuit chips are mounted, is used.

Referring to Fig. 6, with the use of a tape-like sheet which can be rolled up, not only separated sheets as shown in planar sheets, but also a rolled continuous sheet can be provided.

A plurality of electronic circuit chips are mounted on an adhesive tape 61 at predetermined intervals. The adhesive tape is stocked in a rolled condition, and is used by being pulled by a required length. Perforations 62 are formed in the adhesive tape 61 so that a paper piece on which a single electronic circuit chip is mounted can be taken out therefrom.

According this embodiment, even though no electronic circuit chip has yet been mounted to a

desired object, the electronic circuit part can be mounted to the object by cutting off a piece on which a single electronic circuit chip is mounted and then by bonding the same to the object.

5 According to this embodiment, an arbitrary object to which the adhesive tape 61 can be applied, can be mounted thereon with an arbitrary number of electronic circuit chips 41.

10 It is noted that although explanation has been made with the use of the adhesive tape 61 in this embodiment, a seal-like planer adhesive tape may be used, instead of the tape-like sheet.

15 Further, if a cut-off tape 61 can be applied to the object by another means, it is not required that the tape is adhesive.

 Further, the electronic circuit chips should not be limited to one and the same kind, but various kinds of electronic circuit chip can be used.

20 Further, one and the same kind of electronic circuit chips 41 or a plural kinds of electronic circuit chips 41 may be cut off by a number which is not only one but more.

Industrially Usability

25 As mentioned above, according to the present invention, an electronic circuit chip can be mounted on a soft material such as paper while it can be prevented from being broken even though the material is bent or

folded.

Further, according to the present invention, an electronic circuit chip can be simply mounted on the material at an arbitrary position.

FOR "5252550

CLAIMS

1. A method of mounting a planar electronic circuit chip on a flexible sheet together with another planer electric element, characterized by steps of:

selecting the another electric element and the electronic circuit chip so that the planar surface of the another electric element is greater than the planar surface of the electronic circuit chip; and

mounting the another electric element and the electronic circuit chip onto the sheet so that the planer surface of the another electronic element and the planar surface of the electronic circuit chip are located in parallel with the surface of the sheet, and the planer surface of the electronic circuit chip is accommodated within the planar surface of the another electric element as viewed in a direction perpendicular to the surface of the sheet.

2. A method of mounting an electronic circuit chip onto a foldable sheet, characterized in that the electronic circuit chip is mounted to the sheet so that the electronic circuits chip is prevented from being located at a position where a crease is formed when the sheet is folded.

3. A method of mounting a circuit chip on a foldable sheet having a rectangular sheet surface, characterized in that the electronic circuit chip is mounted on the sheet so as to prevent the electronic

circuit chip from being located at least at a position which is obtained by $1/2$, $1/3$ or $1/4$ of the length of longer sides of the sheet surface and which is obtained by $1/2$ of short sides of the sheet surface.

4. A method of mounting an electronic circuit chip as set forth in claim 2, characterized in that the electronic circuit chip is mounted at a position in the vicinity of an edge of the sheet surface.

5. A method of mounting a planer electronic circuit chip on a foldable sheet having a rectangular sheet surface together with another planar electric element, characterized in that setting the planar surface of the another electric element to be slightly smaller than a size of each of rectangular area which are obtained by sectioning the sheet surface by $n \times m$ (where n and m are integers larger than 2), and

mounting the another electric element and the electronic circuit chip on the sheet so that the planer surface of the another electric element and the planar surface of the electronic circuit chip are arranged in parallel with the surface of the sheet, and the planar surface of the another electric element is accommodated within one of the rectangular areas which are obtained by sectioning the sheet surface with $m \times n$, as viewed in a direction perpendicular to the sheet surface, and the planer surface of the electronic circuit chip is accommodated within the planar surface of the another electric element as viewed in a direction perpendicular

to the sheet surface.

6. A method of mounting an electronic circuit chip as set forth in claim 2, characterized in that a long-rod like or a long planar like electric part is mounted on the sheet so that the longitudinal direction of the electric part is coincident with the sidewise direction of the sheet.

7. A method of mounting an electronic circuit chip as set forth in claim 2, characterized in that the sheet is made of paper.

8. A method of mounting an electronic circuit chip as set forth in claim 2, characterized in that the sheet is tape-like.

9. A method of mounting an electronic circuit chip as set forth in claim 7, characterized in that the sheet has a two layer structure, and the electronic circuit chip is mounted between two layers of the sheet.

10. A method of mounting an electronic circuit chip as set forth in claim 7, characterized in that the electronic circuit chip is mounted on the surface of one of two front and rear sheet surfaces of the sheet.

11. A planar electric circuit chip mounted on a flexible sheet, characterized in that the electronic circuit chip has a thickness, a length of the long sides thereof, and a bending strength which satisfy:

$$3PL^2 + 6WL + 6M - \sigma H^2 \leq 0$$

where a force exerted to the electronic circuit chip is

exhibited by equally distributed loads P (N/m^2) per unit area, exerted to the entire planar surface of the electronic circuit chip, and a concentrated load W (N/m) per unit length, is exerted to the free end, in such a case that one of the short sides of the planar surface of the electronic circuit chip is used as a fixed end while the other short side on the opposite side thereof is used as a free end,

where a moment exerted to the electronic circuit chip is exhibited by a moment M (N) per unit length, exerted to the free end in such a case that one of the short sides of the planar surface of the electronic circuit chip is used as a fixed end while the other short side on the opposite side thereof is used as a free end, and

where H (m) is the thickness of the electronic circuit chip;

L (m) is a length of the long sides of the electronic circuit chip; and

σ (N/m^2) is a bending strength of stronger one of a bending strength of the planar another electric element larger than the electronic circuit chip mounted on the planar surface of the another electric element and the bending strength of the electronic circuit chip.

12. A sheet mounted thereon with an electronic circuit chip stated in claim 11.
13. A foldable sheet having a rectangular sheet

surface and mounted thereon with an electric circuit composed of a planar electric circuit chip, a planar capacitor and an antenna, characterized in that the electronic circuit chip is mounted on the sheet so that it is prevented from being located at a position where a crease is created when the sheet is folded in a predetermined folding method, and the another electric element and the electronic circuit chip are mounted on the sheet so that the planar surface of the another electric element and the planar surface of the electronic circuit chip are in parallel with the sheet surface, the planar surface of the electronic circuit chip is accommodated within the planar surface of the another electric element, as viewed in a direction perpendicular to the surface of the sheet, and the antenna is mounted on the sheet so that the longitudinal direction of the antenna is coincident with the sidewise direction of the sheet.

14. A foldable sheet having a rectangular sheet surface, and mounted thereon with an electric circuit having a planar electronic circuit chip, a planar capacitor and an antenna, characterized in that the planar surface of the capacitor has a size which is slightly smaller than that of each of rectangular areas which are obtained by sectioning the sheet surface with $n \times m$ (where n and m are integers larger than 2), and the capacitor, the electronic circuit chip and the antenna are mounted on the sheet so that the

09575360

planar surface of the capacitor and the planar surface of the capacitor are in parallel with the sheet surface, the planar surface of the capacitor is accommodated with one of the rectangular areas obtained by sectioning the sheet surface with $n \times m$, as viewed in a direction perpendicular to the sheet surface, and the planar surface of the electronic circuit part and the contour of the antenna are accommodated within the planar surface of the capacitor as viewed in a direction perpendicular to the sheet surface.

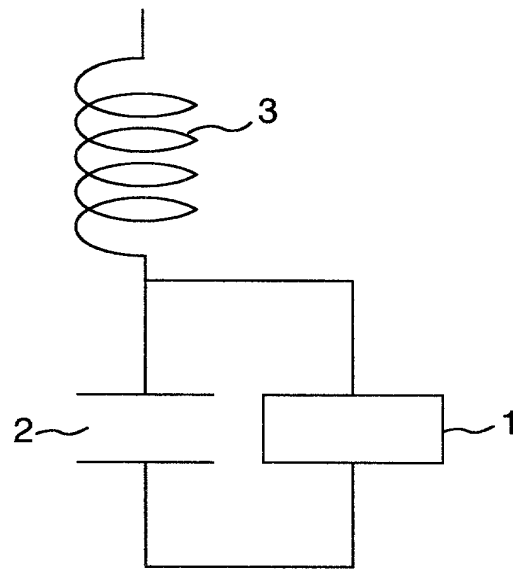
095750 3529550

ABSTRACT

In a method of mounting a planar electronic circuit chip onto a flexible sheet together with another planar electronic element, the electronic circuit part and the another electric element are selected so that the planar surface of the another electric element is greater than the planar surface of the electronic circuit chip, and the another electric element and the electronic circuit chip are mounted on the sheet so that the planar surface of the another electric element and the planar surface of the electronic circuit chip are in parallel with the sheet surface, and the planer surface of the electronic circuit chip is accommodated within the planar surface of the another electric element as viewed in a direction perpendicular to the sheet surface.

FOI b6 b7C

FIG. 1



FOR "E 5885"

FIG. 2a

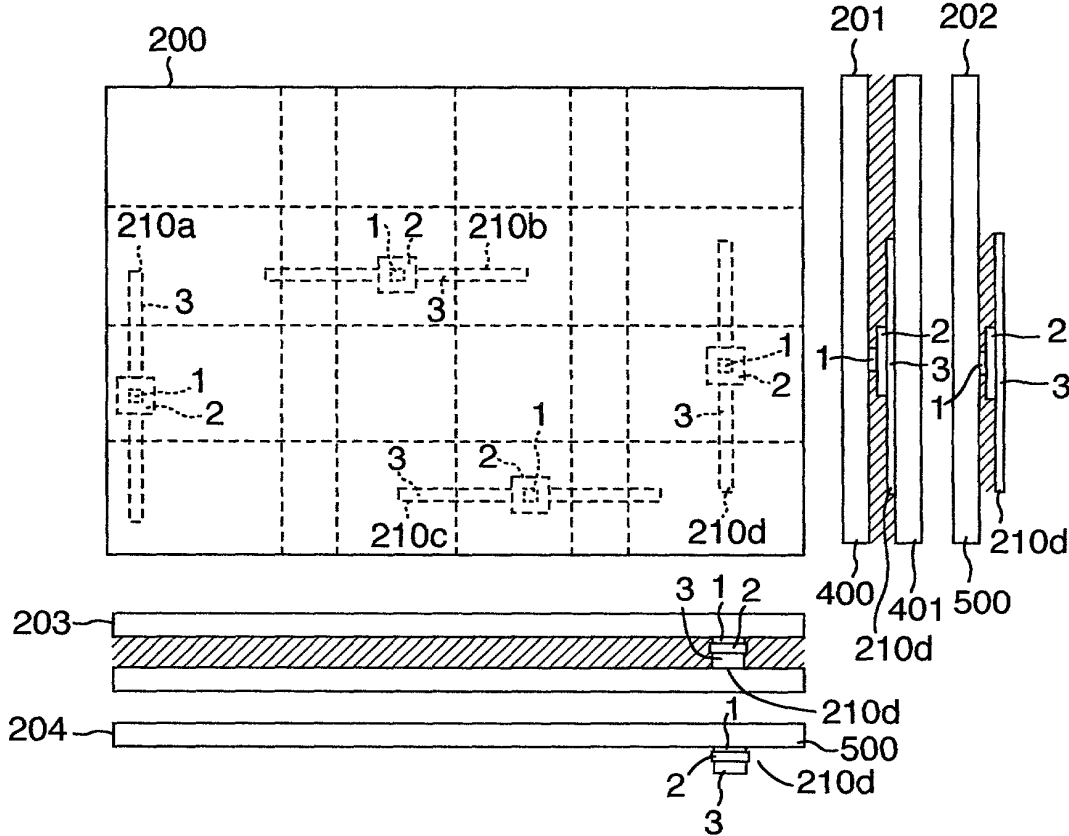
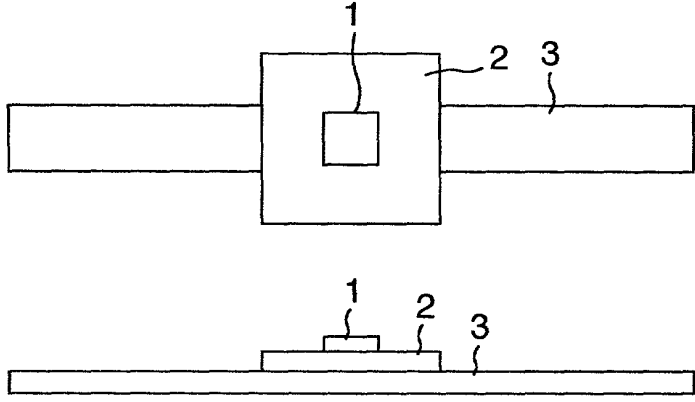


FIG. 2b



09/856758

FIG. 3a

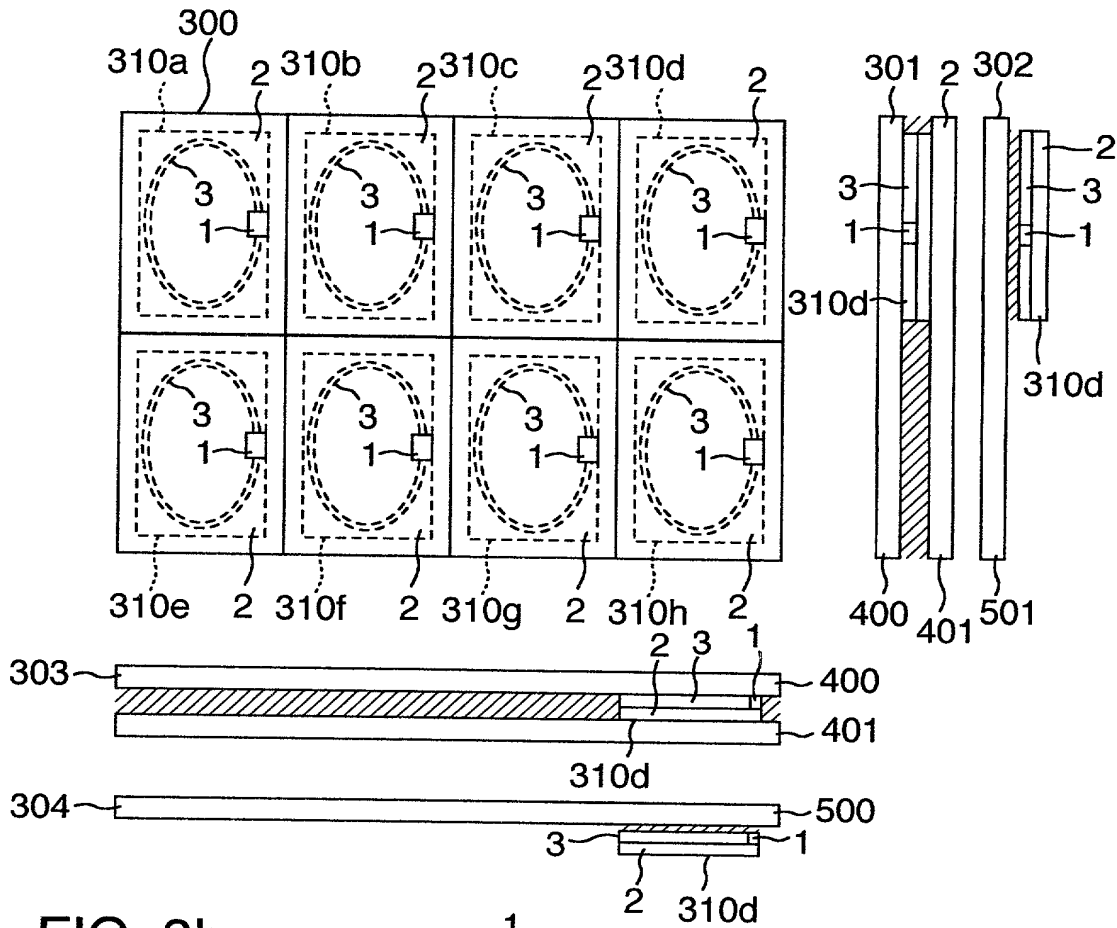
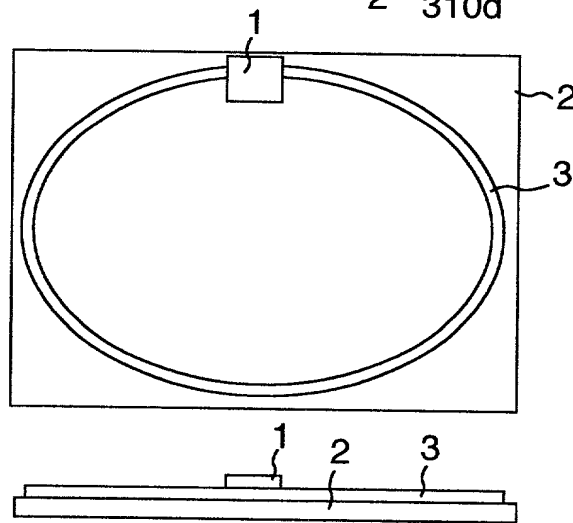


FIG. 3b



POSTNET 8529360

FIG. 4a

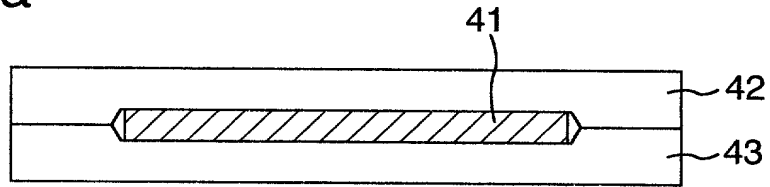


FIG. 4b

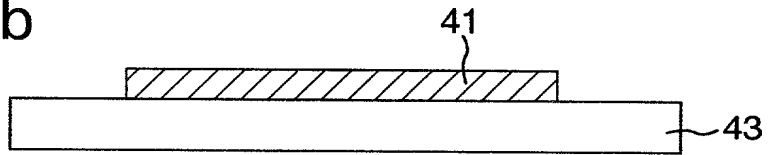


FIG. 4c

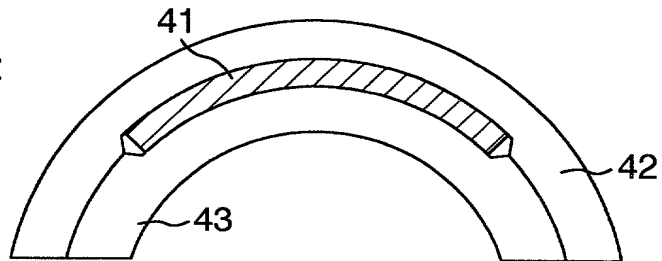


FIG. 4d

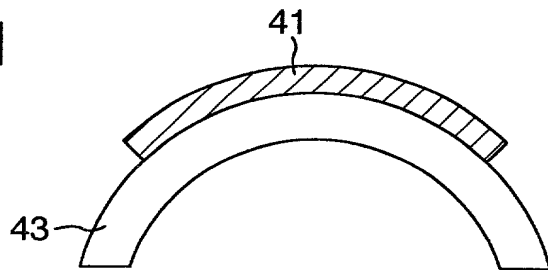


FIG. 4a

FIG. 5

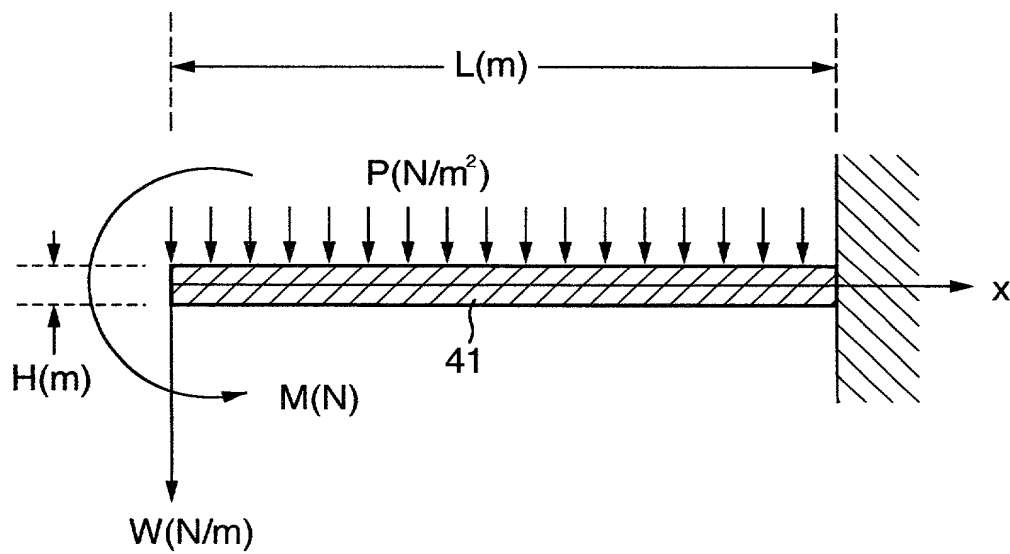
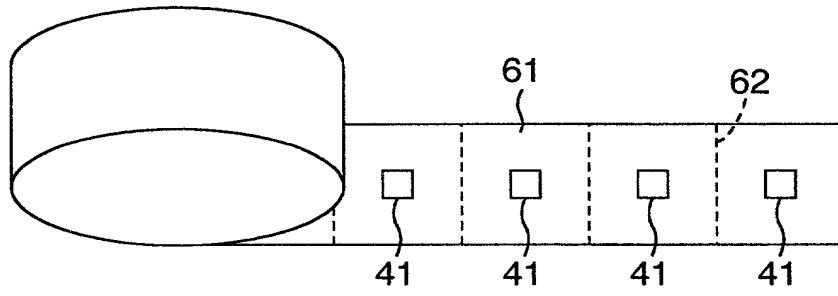


FIG. 6



FOR FIG. 6 856758

E5825

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

METHOD OF MOUNTING ELECTRONIC CIRCUIT

CHIP

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

__月__日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
(該当する場合) _____に訂正されました。

was filed on May 25, 2001
as United States Application Number or
PCT International Application Number
09/856,758 and was amended on
_____(if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

FORM PTO/SB/106

ES 885-01
 (A)

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Japanese Language Declaration
 (日本語宣言書)

私は、米国法典第35編119条 (a) - (d) 項又は365条(b) 項に基き下記の、米国以外の国の少なくとも一カ国を指定している特許協力条約365 (a) 項に基き国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示している。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Priority Not Claimed

外国での先行出願

優先権主張なし

10-339265

Japan

30/November/1998

(Number)
(番号)

(Country)
(国名)

(Day/Month/Year Filed)
(出願年月日)

(Number)
(番号)

(Country)
(国名)

(Day/Month/Year Filed)
(出願年月日)

私は、第35編米国法典119条 (e) 項に基いて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.)
(出願番号)

(Filing Date)
(出願日)

(Application No.)
(出願番号)

(Filing Date)
(出願日)

私は、下記の米国法典第35編120条に基いて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条 (c) に基き権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

PCT/JP99/06595

November 26, 1999

Pending

(Application No.)
(出願番号)

(Filing Date)
(出願日)

(Status: Patented, Pending, Abandoned)
(現況: 特許許可済、係属中、放棄済)

(Application No.)
(出願番号)

(Filing Date)
(出願日)

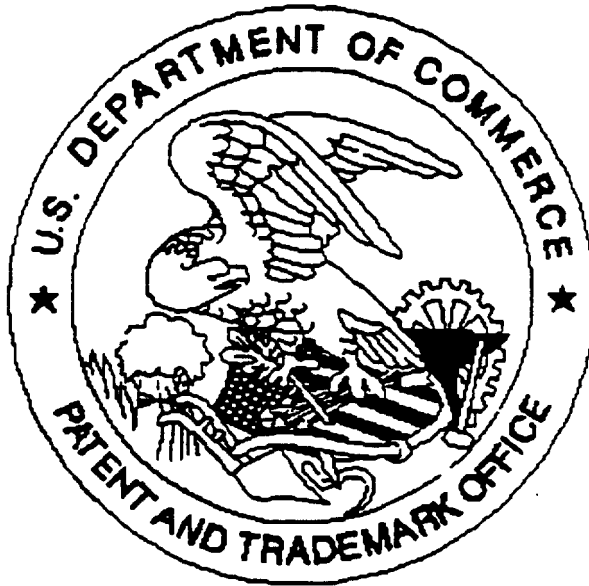
(Status: Patented, Pending, Abandoned)
(現況: 特許許可済、係属中、放棄済)

私は、私自身の知識に基いて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基き、かつ表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基き、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行えば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

FOR OFFICIAL USE ONLY

United States Patent & Trademark Office
Office of Initial Patent Examination – Scanning Division



SCANNED, # 6

Application deficiencies found during scanning:

Page(s) 3, 4, 5 of Declaration were not present
for scanning. (Document title)

Page(s) _____ of _____ were not present
for scanning. (Document title)

Scanned copy is best available.